

<u>Date</u>	<u>Rev</u>	<u>By</u>	<u>History</u>
V0.29	2/7/2025	BMc	<p><u>PDN-3G & -3M Diags only</u></p> <p>1. Fixed power rail connections to OSPI memories by correctly changing name from VDD_MCUIO_1V8 to VDD_IO_1V8 for Grouped PDN scheme.</p> <p><u>PDN-3F Diag only</u></p> <p>2. Added Note 14 to clarify removal of SVS-B & MCU_PWRGRP_IRQn board level net due to removing GPIO Retention low power mode.</p> <p><u>SoC Pwr Seqs:</u></p> <p>1. Corrected power up seq timing diagram to correctly show time btw pwr up seq Time Step #2 vs #3 as only 0.5ms (instead of 1.0ms) per PMIC 133A’s v4 update & as captured in v0.23 changes above.</p>
v0.30	2/19/2025	BMc	<p><u>SoC Pwr Seqs:</u></p> <p>1. Corrected diag to show SOC_PWR_EN (PMIC_ENABLE input) signal asserting low 0.1ms (PMIC’s internal delay T_{DLY0}) before PMIC’s state machine begins executing power down seq by 1st setting MCU_PORz & SOC_PORz low.</p>
v0.31	3/21/2025	BMc	<p><u>SoC Pwr Seqs:</u></p> <p>1. Corrected diag to show both VDD_GPIORET_IO_3V3 & VDD_IO_3V3 min enable time could be ~0.1ms after enabling signals (VDD_MCUIO_3V3 & EN_3V3_IO respectfully).</p> <p>2. An “Immediate Shutdown/Power Down Seq” has recently been approved and will be add to an upcoming data manual version. This simplifies SoC power down to only require both PORz signals to be set low for 1-2us before disabling SoC input supplies in any order.</p>

Power Rails **Control Signals**

← Pwr Rail Names → ← Signals →

Power Rails:

- P2N base
- MCU Only/Safety Island
- GPIO Retention
- DDR_Retention (aka S2R)
- End Product option
- Peripheral loads (SW config'd after boot)
- Debug/Development option

Control Signals:

- General ctrlr & logic
(Italic = SW config'd after boot)
- P2N base ctrlr
- Func Safety
- MCU Only/Island
- GPIO Retention
- DDR_Retention (aka S2R)
- End Product option
- Peripheral comps
- Debug/Development option

Legend:

- P Note items
- P2N On-Chip "Pwr OK" Monitors (OV & UV)
- P2N-UV On-Chip "Pwr OK" Monitors (UV only)
- X Provisioned In-Line Supply Filter
- High-lighted diagram changes

Features Supported (EVM Max Features):

1. SoC performance: Max 2.0GHz clock with SERDES interfaces operational
2. Functional Safety: ASIL-D capable sys w/ isolated Main & MCU power rails (supply FFI)
3. 4x SDRAMs: 32Gb, 4-Die, 32b, 426mT/s, LPDDR4 mode
4. Boot & Mass Flash: Octal SPI or HyperFlash eMMC, UFS
5. Signaling Levels: MCU & Main Dual VIO
6. Low power modes:

(All SoC PN variants: TDA4AP/VP/AH/VH)
(Power Rail & GPIO Mapping Overview)

V0.29 1/27/2025

1. Updated discrete buck's ENABLE input connections to more accurately show the 20k resistor located in-line to voltage translator output.
 2. Updated Note 9, example #2 text & diag to show 20k resistor in-line with buck's ENABLE inputs.
-
1. Corrected a copy & paste error by changing net name "DSRT_PWRGRGP_IRQn" connected to SVS-A's IRQ pin to "MAIN_PWRGRGP_IRQn".
-
1. Added Note 14 to clarify removal of SVS-B & MCU_PWRGRGP_IRQn board level net due to removing GPIO Retention low power mode.

- 2) Load Switches (LDSw) have been used to create VDD_MCUIO_3V3, VDD_GPIORET_3V3 and VDD_IO_3V3 power rails from VCCA_3V3 to provide the following benefits:
 - a) Correct SoC power supply sequencing by using PMIC resources (GPIO signals & power resource outputs) with desired start-up & shut-down timing delays per NVW settings.
 - b) PMIC monitoring of "VCCA Over Voltage" (+5% to +10%) allows PMIC to disconnect 3.3V power rails from SoC I/O condition is detected.
 - c) Enables low power modes (MCU_IO, GPIO_RET & DDR_RET) since the different 3.3V power rails must be disabled independently for different low power modes.
 - d) Connecting VCCA_3V3 directly to SoC 3.3V input supplies is **ONLY** recommended if low power modes are used and a full SoC power up seq is executed any time the VCCA_3V3/VSS_3V3 is energized since partial powering of the SoC for extended time could negatively impact POH reliability.

3.3) PMIC NVM Rev 1 assigned multiple interface signals to GPIO8 with default NVN setting of GPIO_8 = DISABLE. _WDOG function and required interface buffer circuitry, see PROC141E4_SCH for details.

A) DISABLE _WDOG (NVN setting): PMIC latches logic level at GPIO8 NVN on rising edge of PMIC's nRSTOUT = H_MCU_POR2. 1V8 at end of power-up cycle.

a) High level at GPIO8 pin (SW-1/Jmp-1 = closed) directs PMIC to disable Watch-Dog Timer (by setting WDW_PWRHOLD bit to disable timer's long-window time-out) for development/debug.

b) Low level at GPIO8 pin (SW-1/Jmp-1 = open due to PMIC default internal pull-down R) enables Watch-Dog Timer (default setting enables timer's long-window time-out).

B) After system SW boots, SW needs to reassign GPIO_8 = GPI function to operate with P-DN's MAIN_PWRGRGP_IRQ/_IRQn (asserted high or low) signal to allow PMIC to take action if a fault occurs.

- 3.2) PMIC NVM Rev2 & 3 changes are listed below. There are EVM board SCH/BOM impacts, see J78454_EVM_..._PDN-3A v.0.19 for details.
 1. PMIC VCCA input voltage level auto-detection that enables 1 PMIC PN to support PDNis using either 5V or 3.3V.
 2. PMIC internal Watchdog Timer is disabled at start-up. This allows GPIOB function to be used as a PMIC internal configuration control. MCU SW will need to start watchdog timer as part of enabling full FuSa features.

Low = Isolated PDN type directs PMIC to create MCU & SOC power groups; Enables BUCK5 per power up seq (Removes BUCK5 SW write requirement needed in NVM Rev1 above.)
High = Grouped PDN type directs PMIC create only MCU power group; Removes BUCK5 from pwr up seq (Allow SW to reassign Buck5 for peripheral devices that can be enabled after boot)

3.3) PMIC NVM Rev 4 has been optimized for end product production flow by enabling Watch Dog Timer to support FuSa by default, see J784S4_EVM_..._PDN-3A v0.20 & up & PROC141E5_SCH for details.

A) **DISABLE_WDOG (optional):** PMIC latches logic level of **ATP09 pin** at transition from standby to active start-up sequence.

- High level at **GP09 pin** ($V_{DD} - 1\text{mV}$ = closed) drives **PMIC** to disable Watch-Dog timer (by setting **WD_PRRHOLD** to disable timer's long-time-out).
- Low level at **GP09 pin** ($V_{DD} - 1\text{mV}$ = open) drives **PMIC** to enable Watch-Dog timer (by default setting enable timer's long-time-out).

B) **EN_3V3_VDD (required):** After **PMIC** **NVM** initialization, **GPIO0** = **GPIO** function to provide enable & disable control of load switch supplying **VDD0**, **IO3** power rail.

- Disabling the **WDG0R timer** is for development & debug tasks. Applying a pull-up to **R** to disable **WDG0R timer** will result in early enabling of discrete **U0A0** (**VDD0_IO3_V33**), **U0A1** (**VDD0_SVDV**) & **U0A2** (**VDD0_VSDA_V33**). All of these supplies are 3.3V level and are part of the 1st group of supplies to be energized at the start of a power up seq. **SD0** will not be negatively impacted if these 3.3V supplies are enabled ahead of remaining 3.3V supplies sourced from **PMIC** and before the rest of **SC0** supplies begin normal power up seq. during temporary impedance & debouncing activities.

4) GPIO Retention (aka GPIO_RET, IO_RET, IO Wake) low power mode requires:

- A) SoC SW executes command sequence that sets key PMIC register bits in order to enter GPIO_RET low power mode of operation and select the desired wake-up destination state (i.e. Full Active or MCU Only).

1. VDD_GPIORE_WK_DVS supplying MCU's VDD_MCU_WAKEL for MCU's 0.8V wake-up logic

2. VDD_GPIORE_IO_V3V3 supplying MCU's VDDSDHVCU for MCU's 3.3V I/O toggle activity

3. PDM system exts GPIO_RET state upon receiving logic signals on SoC's MCU monitored I/O signals ref to VDDSDHVCU_MCU supply. Then H_MCU_WAKEL [in SoC's open-drain PMIC_WAKEL, active low] signal connected to PMIC_GPIO_4 [in WKPUP default function for Full Active or -WKPUP for MCU only destination state] is asserted and PMIC system master transitions PDM system to targeted wake-up state

4. The Open-Drain Buffer SN74VLC42G07DR1 (pin-18) up to power is OFF) connects PMIC_WAKEL1 to SoC_PWR_WKIN net at discrete open-drain FET node. It is needed to isolate the SoC output buffer from the always on VCCA_V3V3 used as pull-up supply to prevent current bleeding into SoC during low power mode (MCU_DDR_RET) when VDD_GPIORE_V3V3 is typically disabled.

a) DDR Retention (aka DDR_Susp, GPIO = 0, M2N, S2N) low power mode requires:

- a) PMIC Pin to assign **SUSP_6** = Regulator Enable (REGEN) function with an open-drain output buffer type per NVM default settings. The board level net **H_DDR_RET_1VS1** signal is pulled up to **VDDO_DDR_1V1** & connected to **SoC's** **DDR_RET_INP**. When this input is set high, **SoC's** EMIF I/O buffers are set to high-Z state as part of entering **DDR_RET** mode.
- b) **SoC** **SUSP** executes command sequence that sets key PMIC register bits in order to enter **DDR_RET** low power mode of operation and select the desired wake-up destination state [i.e. Full Active or MCU Only].

After entering **DDR_RET** mode, the following power rails will remain energized & all other **SoC** MCU & Main supplies will be shut off to minimize power:

D) PDN system exits DDR_RET upon detecting a CAN_WAKE signal edge toggle on PMIC's GPIO_4 = LP_WKUP1 function per NVM settings that initiates exiting DDR_RET mode & restores Full Active

g) SoC devices come in two types: General Purpose (GP) & High Security (HS). All GP devices can leave the VPP domains unconnected per DM. Pre-programmed HS devices can also leave VPP domains unconnected if no additional FUSE programming is needed. If customer desires capability for in-the-field updates, then on-board FUSE programming will require an additional 1.8V, 150mA I/O. When disabled, this LDO's Vo will need a high impedance output. Recommended PNs: TP75T3101-EF, fixed 1.8V TP75T3118-01 or TLV70100-01. The EN_FUSE_VPP control signal must be sourced from an SoC GPIO for this FDN (due to limited number of PMIC GPIOs). This allows SoC SW to control FUSE VPP voltage level by enabling & disabling dedicated LDO as needed to program High Security SoC Fuses (see SoC FDN for details).

7) PDN shows SoC's VDA_3P3_USB domain supplied from a low noise LDO with a VSYS_5V input as preferred for optimal USB 2.0 data eye mask performance. If USB 2.0 I/F is not used or is only needed for development tasks, then the digital VDD_IO_3V3 rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_3V3 rail to support USB 2.0 I/F removes a discrete LDO & VSYS_5V input but could negatively impact data eye performance due to higher supply noise causing data eye mask violations.

8) PDN shows SoC's Main domain's VDDSHV5 supply being sourced from a dual voltage LDO with a VSYS_5V input as preferred for compliant high-speed SD card operation. If SD card is not used or only standard data rate operation is sufficient, then the digital VDD_IO_3V3 rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_3V3 rail to support SD Card operation removes dual voltage, discrete LDO & VSYS_5V input but will restrict data rates to standard 12Mb/s with VIO = 3.3V.

a) A low voltage transistor with a VGS or VHM max less than 0.76V (-5% supply) up to 0.8V is needed to increase to a 3.3V logic level output. 3x different examples are shown below:

- 1) A discrete FET voltage translator with low VGS threshold below an input min 0.76V. ENVI PR0C1A14E5_7SCHs use discrete FET PNW or low VGS but only an industrial type design.
- 2) A single channel, voltage translator (SNT4AKC145-01) that is automotive AEC-Q100 qualified, grade for -40 to +125°C operation could be used as an alternative. Even valid logic levels are guaranteed for both GPIOs and the Buck-ET output. The SNT4AKC145-01 is available in a 16-pin package.
- 3) The PMIC's GPIOs has NVM default setting that enables a 400k input pull-down. This should be sufficient to keep GPIOs net from "floating" above GPIO's VHM min level when VDDA_D0V8 is disabled which causes the SNT4AKC145-01 output to be tri-stated.

Customer may want to add a pull-down 10k to the board (shown in a 2008 below) just in case the PMIC's internal pull-down is not strong enough to ensure a low logic level.

4) A discrete FET stage is also possible. The PMIC's GPIOs should be able to drive the "MAIN_VREG_800" net to Gnd if Pull-up 20k or 20k are not sufficient.

Examples: #1 - Discrete FETs w/ low VGS #2 – Auto Q1, Single Ch, Voltage Translator w/ low Vth #3 – Same as #2 with additional FETs for open-drain I/F to bi-dir EN/Status pins

Figure 1: Main power supply connection. The diagram shows two circuit options for connecting the main power supply. Option 1 (left) shows a buck converter (SN74AxC145-Q1) connected to VDDA and VDDIO pins, with a 100k resistor between them. Option 2 (right) shows a similar setup but with a 100k resistor between VDDA and VDDIO pins. Both options show the connection of VDDA, VDDIO, and VDD pins to the buck converter output. The input to the buck converter is VDDA, VDDIO, and VDD pins, and the output is connected to VDDA, VDDIO, and VDD pins. The diagram is labeled "MAIN_PWRGRP_IRQn".

(OD buffer /I_{need} for TP56287x-Q1 buck connection using AEC-100 Translator)

10) Worst case analysis for very high thermal use case could result in VCCA_3p3 load current in 15-18A range. This large load current range could lead to a 60 – 72mV voltage drop across Safety FET (Recm'd Part: NVMM54AC05N) for a max Rdson = 4mohm. The TPS22965-01 load switches have max Rdson = 27mohm with 44 max rating resulting in additional max drop of 108mV. SoC's 3.3V supply tolerance is +/-5% or 165mV. Total Rdson drops across Safety FET & Load Switches range from 168 – 180mV which exceed SoC's min voltage limit. For this reason, the Tulpb input voltage will be moved from VCCA_3p3 to VSYS_3p3 since VDD_CPU, AVS & VDD_CORE_0V8 rails account for more than 70% of VCCA_3p3 worst case load currents.

11) If GPIO Retention low power mode is desired, then connect all SVS-B VMON inputs to existing MCU supplies (as shown) sourced from PMIC to enable 1x common PN for SVS-A & -8 while avoiding false positives on "unconnected" VMONs. If an end product does not need GPIO Retention low power mode, then the 3x following components can be removed from the PDN: LDO-C, LDO-B & SVS-B. Group the SoC input supplies according to the "PDN Features for Isolated Power Rails" table shown below using the "Standard Operation & MCU Only" assignments row.

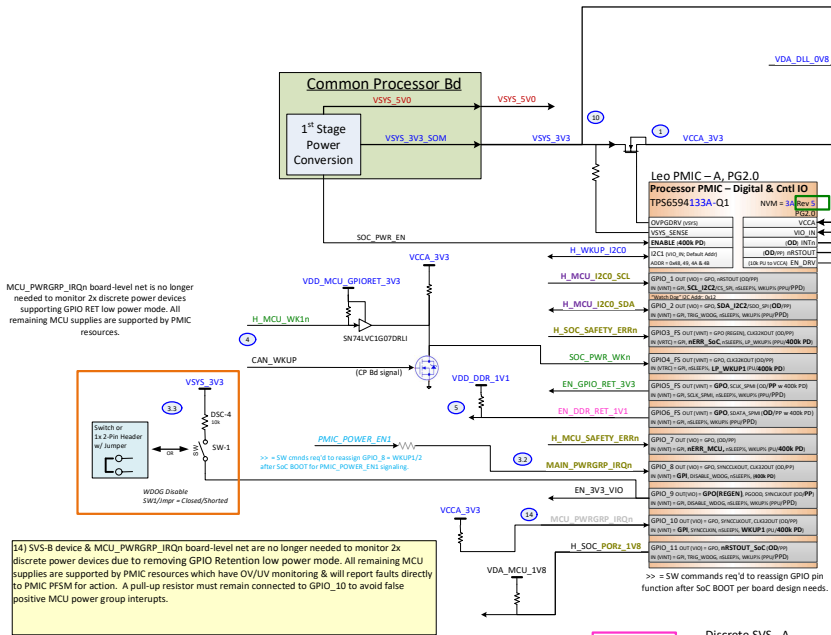
(2) The OR gate function enabling the discrete LDO supplying 1.8V to LPDDR4 VDD1 (internal bias voltage) needs to revert back to original discrete FET OR gate circuitry (see PROC141E2_SCH or snap-shot below). Reason for reverting is due to the OR gate needing a max input voltage threshold less than 1.05V (-5% of 1.1V) since the EN_DDR_RET_1 input signal is sourced from an open-drain PMIC. GPIO with PU resistor to VDD_DDR_1V1 supply with +/-5% supply tolerance. In addition, the OR gate needs to remain energized during DDR Retention low power mode when only VDD_DDR_1V1 & VDD1_DDR_1V8 rails remain energized. Therefore, the OR gate supply must use V515_3V3 or VCCA_3V3 input supply that remains on in OR Ret hold mode. The single logic gate IC (SN74LVC1G97-Q1) used for enabling other power resources interposed to 3.3V signaling levels can not be used with 1.1V signaling since its max input voltage threshold for 3.3V supply is ~2.2V.

Original discrete FET OR gate circuit used in PROC141E2_SCH:

(3) The Safety Voltage Supervision (SVS-4 & SVS-8) actively connections need to be changed from "Always On" VCCA_3V3 (+VVS_3V3) to "PMIC controlled" power rail so that resetting of an asserted IRQn signal by power cycling SVDS devices. During functional testing, it was discovered that an SVS's asserted IRQn could not be reset if PMIC processor I2C comm with SVS devices is lost. This will happen if a MCU Power Error occurs (i.e., fault on a MCU supply) since this will cause the PMIC PSM1 to transition the system to the desired Safe Recovery state (powers down all SOC supplies). However, if the SOC PSM's input voltage VCCA_3V3 remains energized, then the energized SVDS would maintain an asserted IRQn and the system will not be able to execute a cold boot attempt due a previously asserted IRQn. To prevent this situation, the SVS devices must be configured to allow the PMIC to control the power rails. When the SVS devices are configured to "Always On" VCCA_3V3 supply connections with a PMIC controlled power rail (VDD_MCU_0V3), the SVS devices will have a power cycle event upon entering the Safe Recovery state (per table below). If a fault occurs on a Main domain supply, the PMIC will transition the system to MCUS Only state which allows I2C comms to evaluate & potentially log the fault source. The MCU can use I2C comms to clear an asserted IRQn if a system cold boot attempt is desired.

The SVS devices will also respond to a fault rate since a fault might clear if it's due to a random noise event or temperature dependence. The SVS device's "Active" Input connection will need to be connected to VDD_MCU_0V3 supply connection as well as VCCA_3V3 supply connection is enabled as part of the SOC power up seq. This avoids driving a high logic signal into an unenergized device.

PDN State:	Active	MCU Only	Safe Recovery
	Main supplies = ON	Main supplies = OFF	Main supplies = OFF
	MCU supplies = ON	MCU supplies = ON	MCU supplies = OFF
	SVS-A = ON	SVS-A = ON	SVS-A = OFF
	SVS-B = ON	SVS-B = ON	SVS-B = OFF

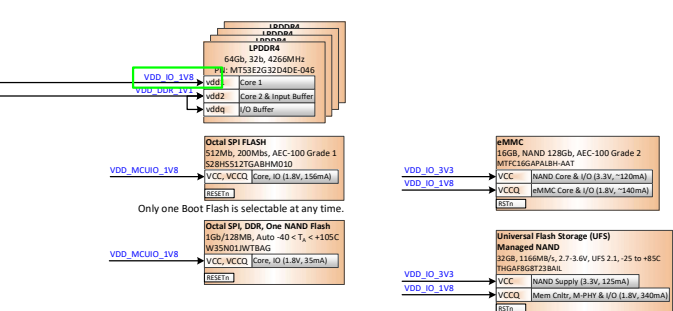
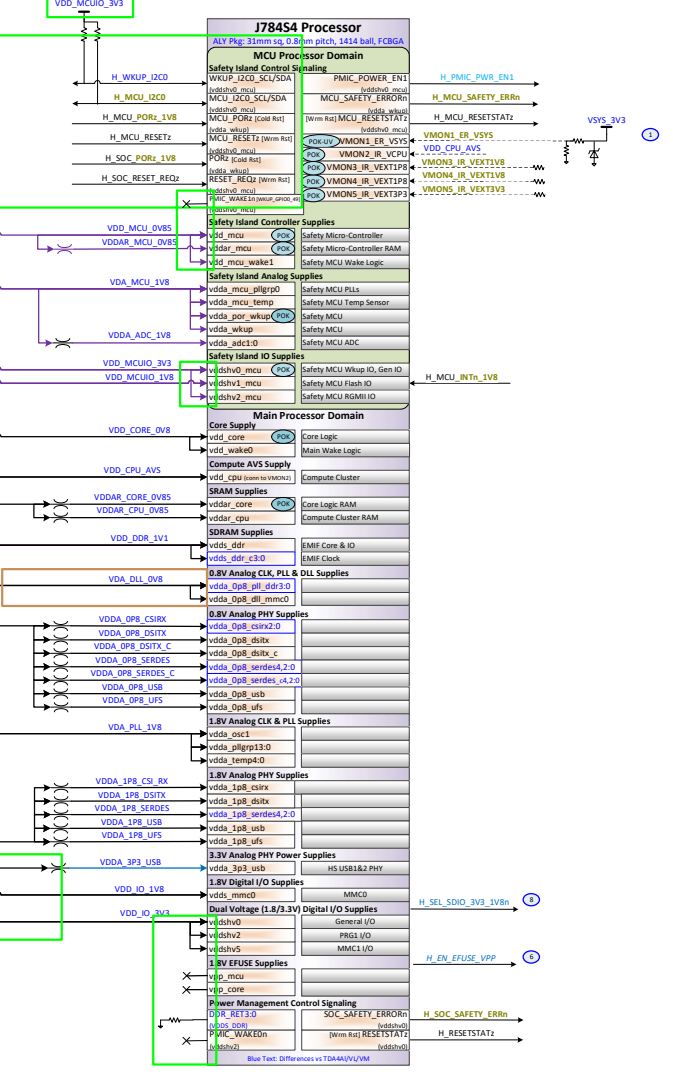
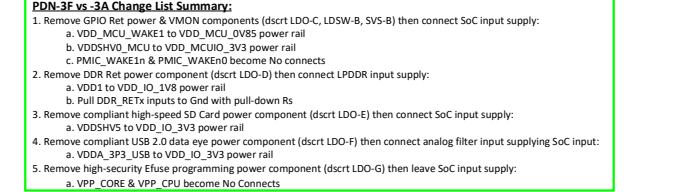
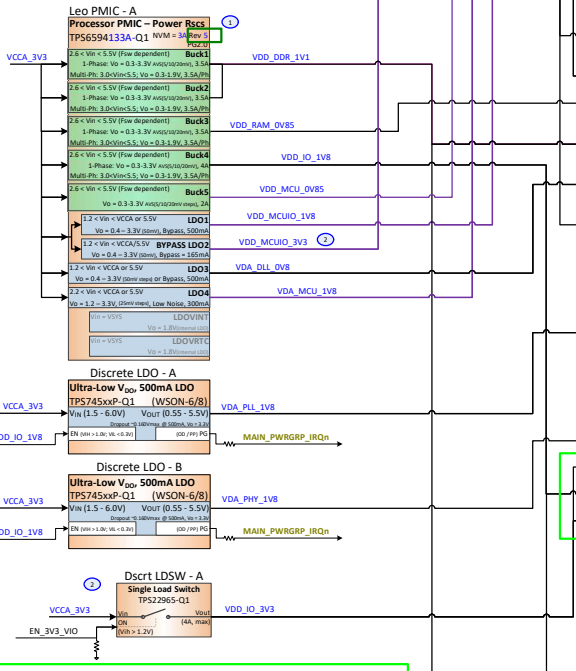
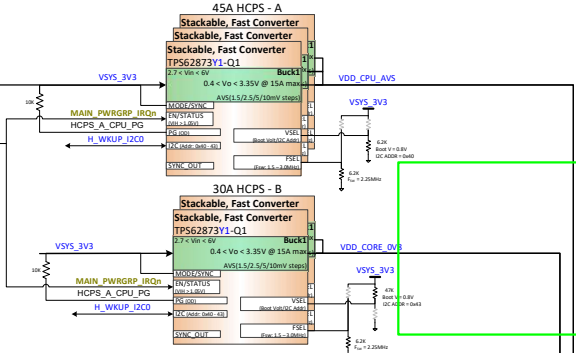


Modular PDNs support Flexible Feature Set Reductions		
Feature Removals	Power Resource & Power Rail Removals	New Supply Mappings
HS SoC EFUSE Programming	Discrete LDO VPP_EFUSE_V18	Soc: VPPs → No connects
Compliant, USB 2.0 data eye	Discrete LDO VDDA_USB_V33	Soc: VDDA_USB_18U → Filtered VDDO_1V33
Compliant, High-Speed SD Card	Discrete LDO VDD_SD_1V8	Soc: VDDSHVS → VDDO_1V33 or VDDO_1V8
DDR Retention low power mode	Discrete LDO VDDO_DDR_V18	LPDDR4: VDDO1 → VDDO_1V8 or VDDO_1V8
MCU GPIO Retention low power mode	Discrete LDO VDD_MCU_GPIORET_V18	Isolated MCU & Main PDN Schemes: Soc: VDD_MCU_WAKES1 → VDD_MCU_DVBS
		Grouped MCU & Main PDN Schemes: Soc: VDD_MCU_WAKES1 → VDD_CORE_V18
	Discrete L2SW VDD_MCU_GPIORET_V33	Isolated MCU & Main PDN Schemes: Soc: VDDSHV0_MCU → VDD_MCU18_V33 or VDD_MCU18_V18
		Grouped MCU & Main PDN Schemes: Soc: VDDSHV0_MCU → VDDO_1V33 or VDDO_1V8
Main GPIO Retention low power mode	Discrete SVS VDD_GPIORET_V18	PMIC: GPIO_10 pulled-up to VCCA_V33 Soc: VDD_WAKES0 → VDD_CORE_V18
	Discrete L2SW VDD_GPIORET_V33	Soc: VDDSHV2 → VDDO_1V33 or VDDO_1V8
	Discrete SVS	PMIC: GPIO_10 pulled-up to VCCA_V33

SoC Input Supply to Power Rail Groupings vs PDN Low Power Mode Features									
PDN Features		Isolated MCU & Main PDN Power Rails							
	VDD_MCU_0v85	VDD_CORE_0v8	VDD_MCU0_1v3	VDD_IO_1v8	VDD_IO_1v3	VDD1_DDR_1v8	VDD_GPIORET_0v8	VDD_GPIORET_1v3	
Standard Operation	vdd_mcu								
MCU Only	vddar_mcu	vdd_core	vddshv2_mcu	vdd1_mmc0	vddshv0				
	vdd_mcu_wake1	vdd_wake0		DDR_vd1	vddshv2				
	vdd_mcu								
DDR Retention	vdd_mcu_wake1	vdd_core	vddshv0_mcu	vdd1_mmc0	vddshv2				
	vddar_mcu	vdd_core				DDR_vd1			
I/O Retention-MCU & Main			vddshv2_mcu	vdd1_mmc0	vddshv0		vdd_mcu_wake1	vddshv0_mcu	
	vddar_mcu			DDR_vd1			vdd_wake0	vddshv2	
I/O Retention-MCU		vdd_core	vddshv2_mcu	vdd1_mmc0	vddshv0		vdd_mcu_wake1	vddshv0_mcu	
	vddar_mcu			DDR_vd1	vddshv2				
I/O Retention-Main	vdd_mcu_wake1	vdd_core	vddshv0_mcu	vdd1_mmc0	vddshv0				
			DDR_vd1				vdd_wake0	vddshv2	

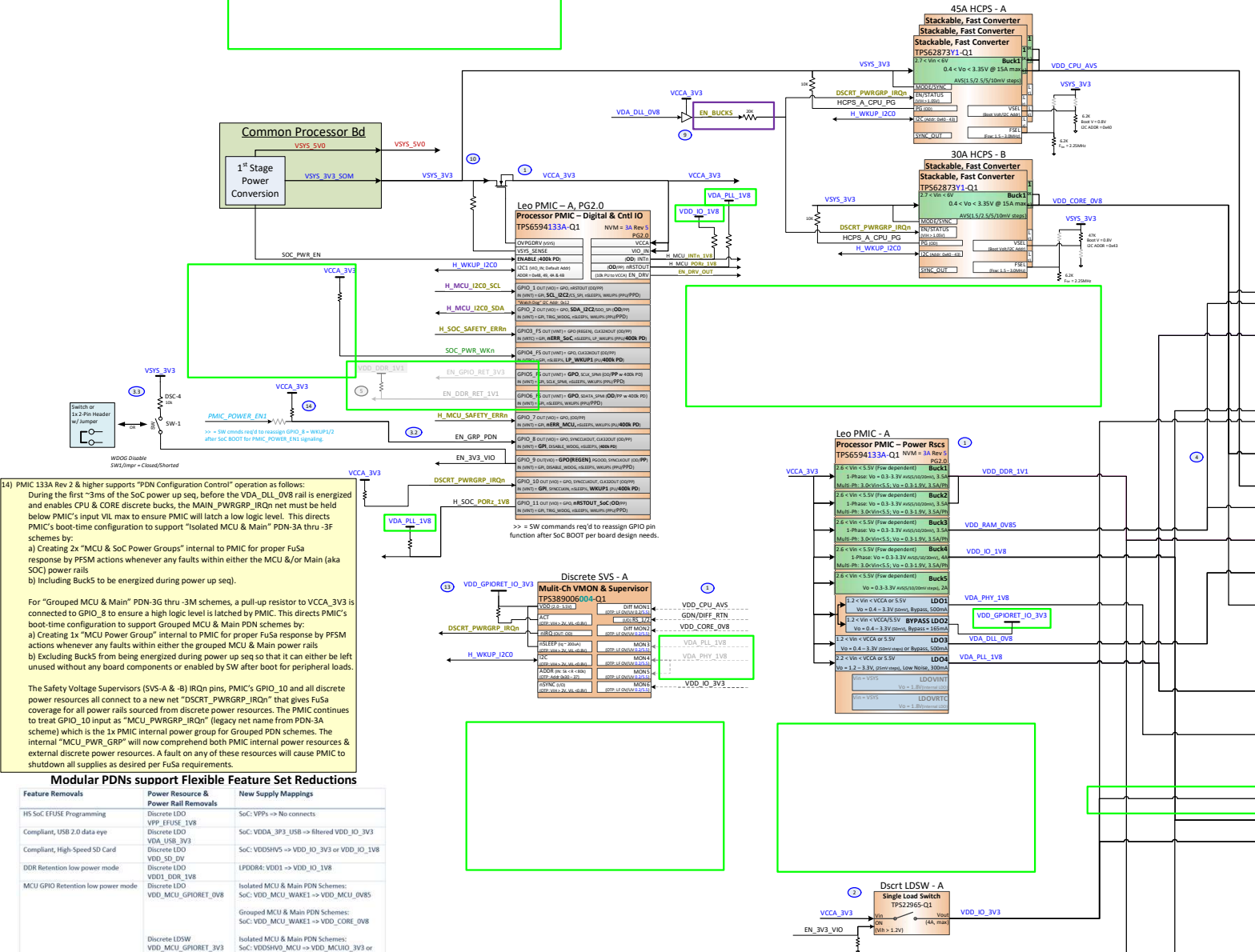
Notes:

- 1) Power rail names shown in "ALL CAPITAL LETTERS"
- 2) SoC input supplies shown in "all lower case letters"



Only one Boot Flash is selectable at any time.

Power Rails	Control Signals	
<p>PCU base</p> <p>MCU Only/Safety Island</p> <p>GPIO Retention</p> <p>DDR_Retention (aka S2R)</p> <p>End Product option</p> <p>Peripheral loads (SW config'd after boot)</p>	<p>General ctrl'l & logic (<i>Italic = SW config'd after boot</i>)</p> <p>PDn base ctrl'l</p> <p>Func Safety</p> <p>MCU Only/Island</p> <p>GPIO Retention</p> <p>DDR_Retention (aka S2R)</p> <p>End Product option</p> <p>Peripheral comps</p> <p>Debug/Development option</p>	<p>Note items</p> <p>On-Chip "Pwr OK" Monitors (OV & UV)</p> <p>On-Chip "Pwr OK" Monitors (UV only)</p> <p>Provisioned In-Line Supply Filter</p> <p>High-lighted diagram changes</p>

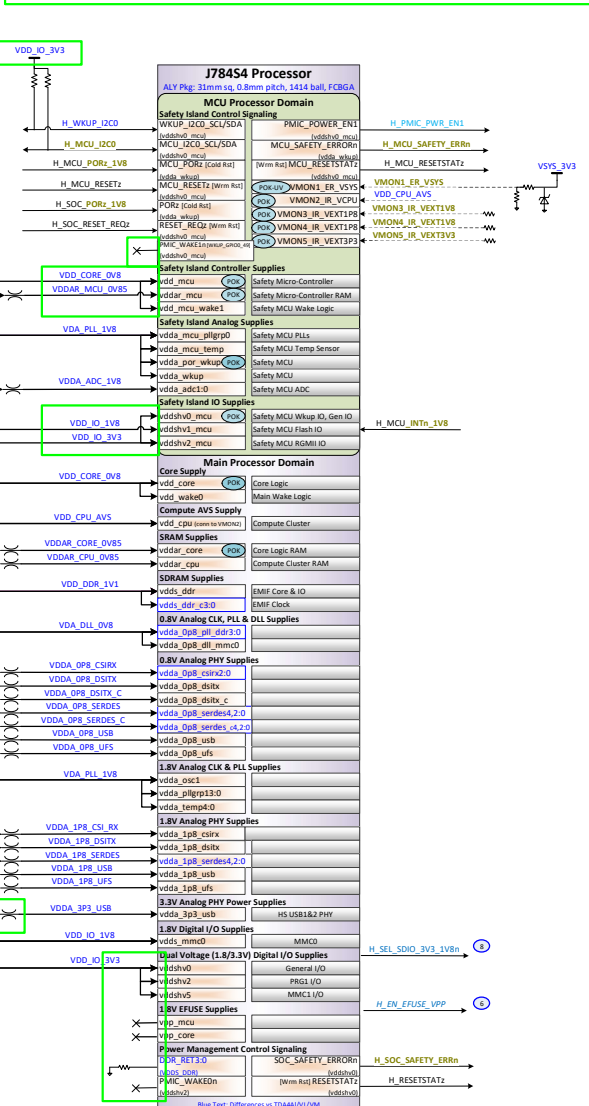
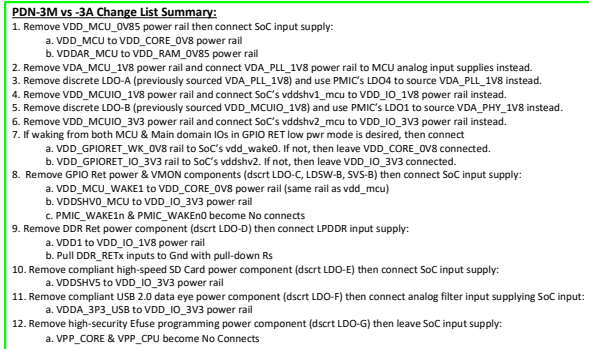


		VDD_MCUIO_1V8
		Grouped MCU & Main PDN Schemes: SoC: VDDSHV0_MCU → VDD_IO_3V3 or VDD_IO_1V8
Main GPIO Retention low power mode	Discrete SVS Discrete LDO VDD_GPIORET_0V8	PMIC: GPIO_10 pulled-up to VCCA_3V3 SoC: VDD_WAKED0 → VDD_CORE_0V8
	Discrete L2SW VDD_GPIORET_3V3	SoC: VDDSHV2 → VDD_IO_3V3 or VDD_IO_1V8
	Discrete SVS	PMIC: GPIO_10 pulled-up to VCCA_3V3

2) SOL input supplies shown in all lower case letters

(Power Rail & GND Mapping Overview)

- Updated discrete buck's ENABLE input connections to more accurately show the 20k resistor located in-line to voltage translator output.
 - Updated Note 9, example #2 text & diag to show 20k resistor in-line with buck's ENABLE inputs.
-
- Fixed power rail connections to OSPI memories by correctly changing name from VDD_MCUIO_1V8 to VDD_IO_1V8 for Grouped PDN scheme.



Only one Boot Flash is selectable at any time.

MMC
GB, NAND 128Gb, AEC-100 Grade 2

TFC16GAPALBH-AAT

CCQ	eMMC Core & I/O (1.8V, ~140mA)
-----	--------------------------------

Time

Universal Flash Storage (UFS)

Managed NAND
GB, 1166MB/s, 2.7-3.6V, UFS 2.1, -25 to +85C

CC	NAND Supply (2.3V, 125mA)
----	---------------------------

CCQ	Mem Cntr, M-PHY & I/O (1.8V, 340mA)
-----	-------------------------------------

T20

TPS6594133A NVM | Revision History

Revision	Release Date	Comments
0.0	April 25, 2022	
1.0	August 8, 2022	
2.0	October 10, 2022	TI J784S4 EVM Samples
3.0	December 15, 2022	RTM'd in January 2023
4.0	Only released in sample units	
5.0	March 1, 2024	PCN released and all parts received after March 1st , 2024 contain Rev 5

Rev	Change	Impact of Change
2.0	VCCA input voltage level auto-detection	Enables 1x PMIC PN to support PDNs with VCCA voltage of 5V or 3.3V
	Watchdog Timer disabled	<ul style="list-style-type: none">GPIO8 used for PMIC config controlMCU SW will need to start watchdog timer as part of enabling full FuSa features
	GPIO8 logic level latched before 3ms time step of power up sequence & directs PMIC to configure internal resources: <ul style="list-style-type: none">Low = Creates 2x power groups; Enables BUCK5 per power up seqHigh = Creates 1x power group; Removes BUCK5 from power up seq	<ul style="list-style-type: none">Isolated MCU & Main PDNs (3A to 3F) need 2x power groups, use Buck5 for VDD_MCU_0V85 rail & connect MAIN_PWRGRP_IRQn to GPIO8 for discrete power resource monitoring.Grouped MCU & Main PDNs (3G to 3M) need 1x power group, removes Buck5 from pwr up seq (Buck5 can be reassigned by SW config to supply a peripheral rail after SoC & SW boot-up) & connects GPIO8 to pull-up resistor to₃, set logic high.

Rev	Change	Impact of Change
2.0	Removed anyZota sequence	PMIC OTA preparation sequence is no longer available. Unused during normal operation.
	Fixed GPIO10 response during normal operation	Prevents PMIC from getting stuck after MCU_PWRGRP_IRQn triggers a recovery attempt
3.0	Adjusted internal setting for improved BUCK reliability	No impact to function

Rev	Change	Impact of Change
4.0	Watchdog enabled by default with 1 sec long window	MCU SW must boot and configure watchdog within 1 second of nRSTOUT going high
	Change default GPIO9 function from GPIO to WD_DISABLE	GPIO9 starts as an input to set WD_PWRHOLD bit, then changes to an output. In Development: Customer has <i>option</i> to use external PU resistor to set WD_PWRHOLD =1 In End Equipment: No impact to function
	TO_ACTIVE sequence has 500us delay between LDO3 and BUCK5	In systems with split power groups, PMIC BUCK5 powers up fully before PMIC LDO3. Overall sequence time remains the same.
	LDO2 OV/UV Threshold changed from 5% to 10%	When used as 3.3V load switch, PG Window will match that of VCCA. Customer can tighten after boot.

*Error found EN_I2C_CRC sequence, only on Rev4

Rev	Change	Impact of Change
5.0	Watchdog Long Window set to 13 minutes.	MCU SW must boot and configure watchdog within 13 minutes of nRSTOUT going high
	Fixed EN_I2C_CRC sequence error	MCU can use I2C_2 FSM Trigger to enable I2C CRC

Rev 4 I2C_CRC_EN Error and Workaround

- What:** Setting I2C_2 FSM Trigger high to enable the I2C CRC does not work on Rev 4 of TPS6594133A
- Why:** Implementation of changes for watchdog and GPIO9 for disable watchdog pushed NVM over the memory limit
- Affected Revisions:** Only Rev 4 is impacted. This was fixed in Rev 5
- Software Workaround:** Instead of using the I2C_2 FSM trigger, please use SW workaround described on next page

Item	Change	Impact
1	Watchdog enabled by default with 1 sec long window	MCU SW must boot and configure watchdog within 1 sec of nRSTOUT (SoC's MCU_PORz) going high
2	Change GPIO9's default NVM function from GPI to WD_DISABLE	GPIO9 starts as an input to set WD_PWRHOLD bit, then changes to an output. In Development/Debug: Customer has <i>option</i> to use external PU resistor to disable WD Timer by setting WD_PWRHOLD =1 In End Equipment: WD Timer enabled by default
3	TO_ACTIVE sequence adds 500us delay to LDO3 enable	Adds timing margin to ensure BUCK5 (SoC's VDD_MCU_0V85) powers up fully before Tulip buck (SoC's VDD_CORE_0V8) that is enabled by LDO3
4	LDO2 output OV/UV Threshold changed from 5% to 10%	When used as 3.3V load switch, PG Window will match that of VCCA since both are supplied by VSYS_3V3 input voltage from pre-regulator. Customer can tighten after boot.

Rev	Change	Impact of Change
1.0	GPIO Retention Entry/Exit Handling – If Wake signal triggers while being armed, PMIC will enter Retention and then immediately exit.	Prevents PMIC from getting stuck in Retention
	Power Down Sequence Timing Changes -Updated power down seq of VDA_DLL_0V8 to shift disabling from 2.5ms to 1.0ms due to ~1ms delay in VDA_DLL_0V8 RC discharge before VDD_CPU_AVS & VDD_CORE_0V8 are disabled by VDA_DLL_0V8 dropping below 0.6V FET Von threshold. -Updated power down seq of VDD_MCU_0V85 to shift disabling from 2.5ms to 2.0ms to ~align with disabling of VDD_CPU_AVS & VDD_CORE_0V8.	Overall sequence time remains the same. Better power down seq when using discrete component rails to align with J7 SoC DM recommended seq.
	At startup, all PMIC power resources/rails mapped to a single MCU_PWR_ERR group	<ul style="list-style-type: none">Enables 1x PMIC PN to support both Grouped & Isolated PDN board designsGrouped MCU & Main PDNs (3G to 3M) need 1x PMIC power group to enable fault on any monitored rail to cause an orderly shutdown.Isolated MCU & Main PDNs (3A to 3F) will need MCU SW to create 2x power groups (MCU & Main) by writing 0x1E to PMIC register 0x44

J784S4 EVM Leo + 2x High-Current Pwr Stages(HCPS) PDN-3A

Legend:

System Elapsed Times
Device Timing Parameters
Board Power Rail – Active State / Control Signal Nets / SoC voltage domains
Board Power Rail – GPIO Retention / Control Signal Nets / SoC voltage domains
Board Power Rail – DDR Retention / Control Signal Nets / SoC voltage domains
Discrete Power Component
PMIC Power Component
NVM Settings: (Pwr Rsrc, Current Capacity, Boot Voltage, Delay After Enable [us], Slew Rate [mV/us])
(GPIO# = Function, Ref Voltage, Output Buffer Type, Logic @ T=0, Logic @ Elapsed time [us])

\$ Indicates PMIC Control Signal & Power Resource and Board Power Rail counts that transition during power sequences

= Boolean *OR* logic & = Boolean *AND* logic

Verified per NVM file



Leo PMIC-A, PN TPS6594133ARWERQ1 (TI PN ID = 1, MP Buck Rails = 3, PG2.0 NVM ID = 3A Rev 4 or higher)

HCPS-A & B, Tulip PN TPS62873Y1QWRXSQRQ1 (15A PN ID = 3, Jacinto7 Family ID = Y1)

Safety Voltage Supervisor, PN TPS389006004RTERQ1 (OTP ID = 004 = new common PN for use with Jacinto7)

J784S4 PDN-3A scheme)

Rev Date

V0.23 10/26/2023

By Desc

BMc

1. Increase time btw pwr up seq Time Step #2 vs #3 to add 0.5ms margin btw VDD_MCU_0V85 vs VDD_CORE_0V8 for worst case per SoC errata i2406

V0.23b 10/27/2023

BMc

2. Updated PMIC PN NVM revision from v2 to v4

V0.23c 12/06/2023

BMc

3. Added new power up seq constraints list for quick reference as needed to align with Errata i2406 "IO Glitches during Pwr Up Seqs"

v0.29 2/07/2025

BMc

1. Corrected power up seq timing diagram to correctly show time btw pwr up seq Time Step #2 vs #3 as only 0.5ms (instead of 1.0ms).

v0.30 2/19/2025

BMc

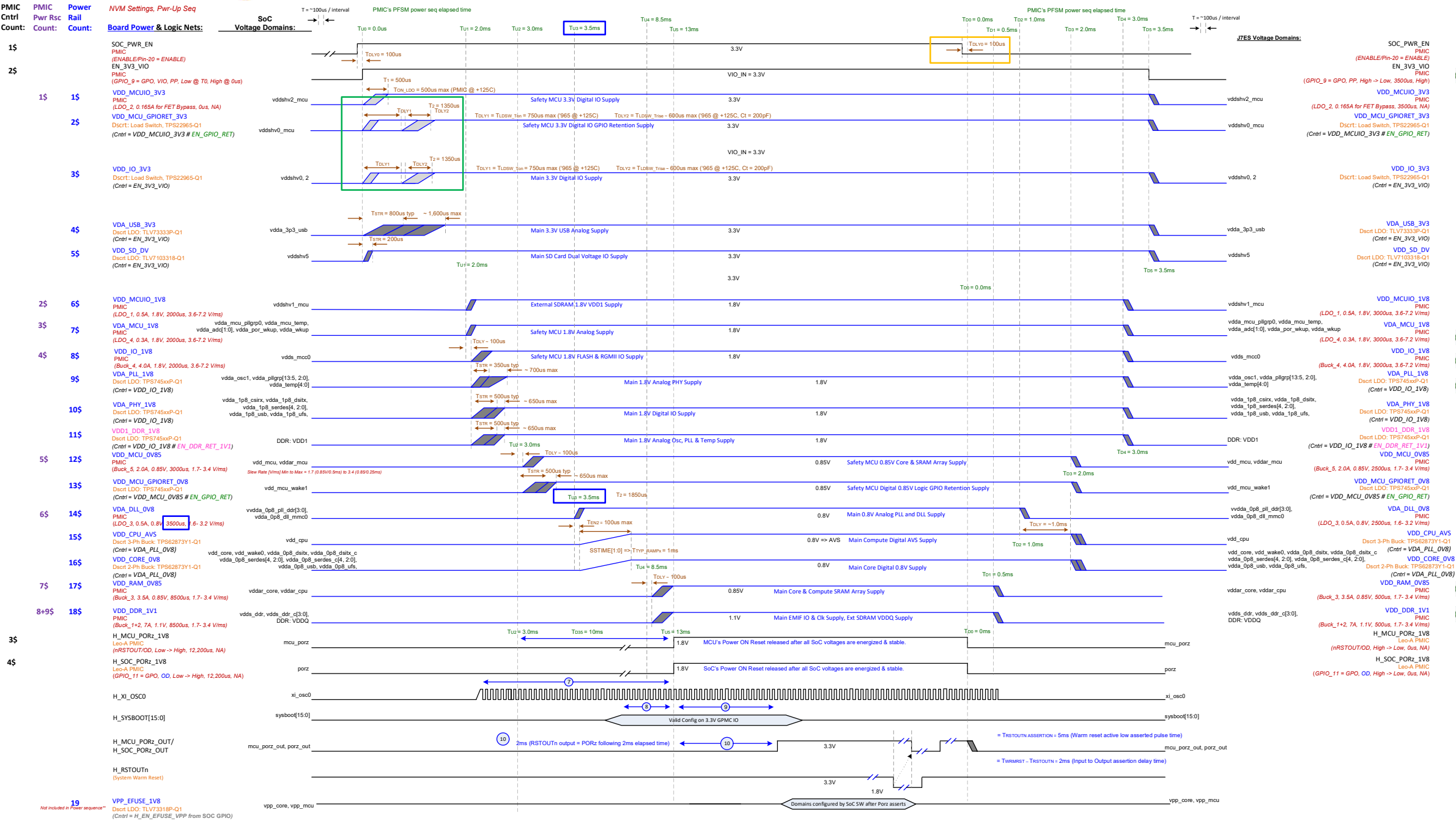
1. Corrected diag to show SOC_PWR_EN (PMIC_ENABLE input) signal asserting low 0.1ms (PMIC's internal delay T_{OLV0}) before PMIC's state machine begins executing power down seq by 1st setting MCU_PORz & SOC_PORz low.

v0.31 3/21/2025

BMc

1. Corrected diag to show both VDD_GPIORET_IO_3V3 & VDD_IO_3V3 min enable time could be ~0.1ms after enabling signals (VDD_MCUIO_3V3 & EN_3V3_IO respectfully).

2. An "Immediate Shutdown/Power Down Seq" has recently been approved and will be add to an upcoming data manual version. This simplifies SOC power down to only require both PORz signals to be set low for 1-2us before disabling SoC input supplies in any order.



1.4.1 Power rails

NOTE: K3W1 devices are intended for use with low-cost PMIC. Depending on system needs, certain supply rails may be ganged. Power sequencing requirements are generally high to low and will follow a recommended sequence implemented by the PMIC.

The architecture will support any power sequence (with exception of array and VDDIO IC supplies, see exception descriptions below), but validation will be limited to those enforced by PMIC. External voltage supervisors (discrete or on PMIC) must be used to provide PWR reset to the device. On-chip PWR circuitry provides redundant supply monitoring (in addition to any PMIC monitoring) for safety applications.

Power sequencing exceptions:

Due to specific analog IP restrictions, several power sequencing restrictions are required as follows:

RAM array supplies (D'es_arch.asp.41):

During active power ramp, the core supply must always lead the corresponding array supply during ramp-up and must lag the corresponding array supply during ramp-down such that VDDIO (core) < VDDAR (array).

To meet lifetime reliability specs, during any other uncontrolled ramp down, ensure that the array supply (VDDA) is not actively driven when the corresponding core (VDDIO) is < 200mV.

DDR IO supplies (D'es_arch.asp.64):

During active power ramp-up, the core supply must ramp to valid level before beginning DDR IO supply ramp (1.1V, 0.6V).

During active power ramp-down, the DDR IO supplies (1.1V/0.6V) must ramp down below DDR logic VIL levels before the core supply begins to ramp down below valid level.

J7 SoC Errata Item i2406 | Power Sequence Limitations

• Errata i2406 summary

– In order to prevent random IO signal pulses & potential IO drive contention during the power up sequence

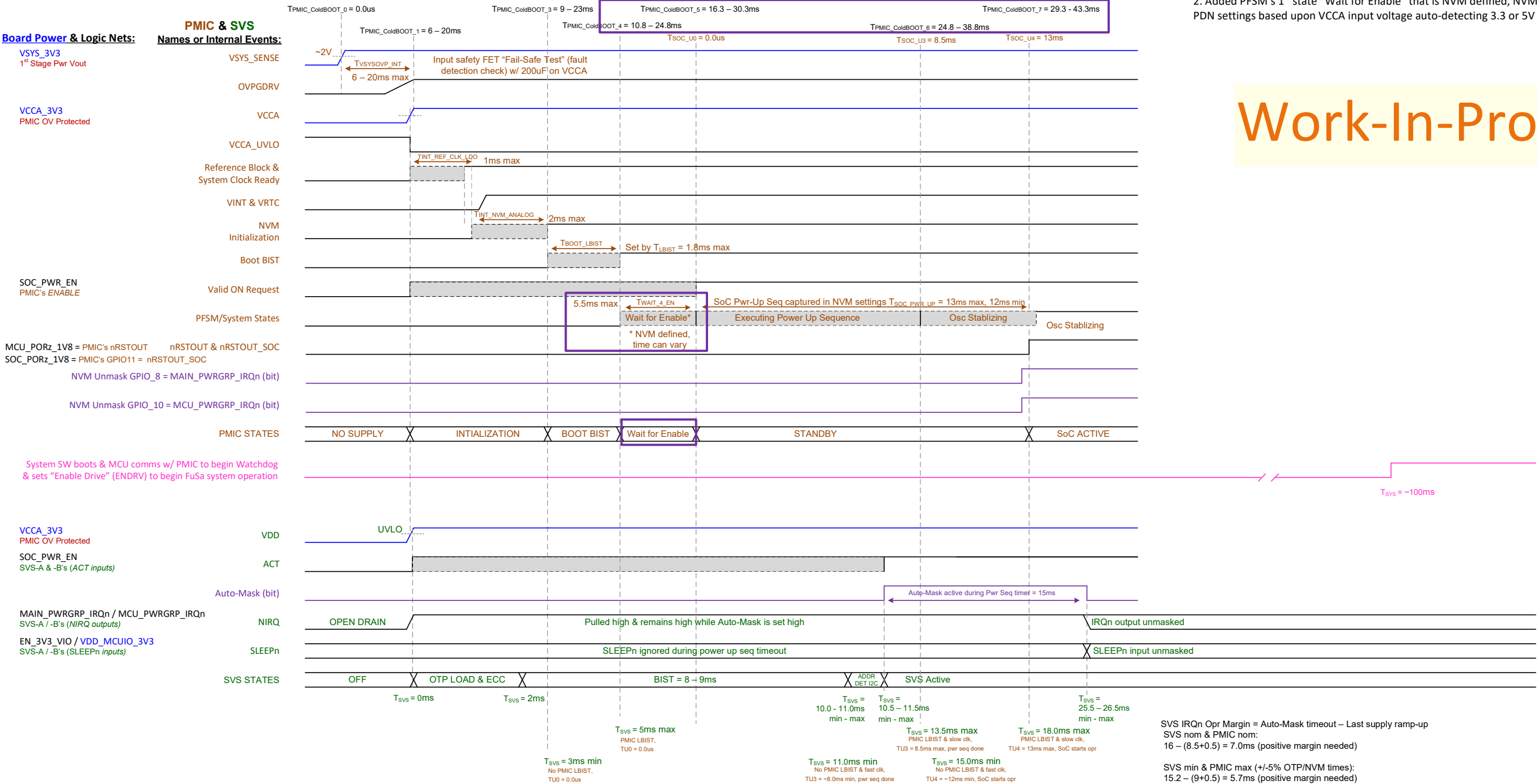
• New power-up seq constraints

- VDD_CORE must ramp-up before or from same power resource supplying VDD_WAKE0.
- VDD_MCU must ramp-up before or from same power resource supplying VDD_MCU_WAKE1.
- VDD_MCU should ramped-up based upon the Vnom level and power resource as follows:
 - Vnom = 0.8V & same 0.8V power resource supplying all 0.8V core level supplies (VDD_CORE, VDD_WAKE0 & VDD_MCU_WAKE1) should ramp VDD_MCU simultaneously with all 0.8V core level supplies.
 - Vnom = 0.85V & independent 0.85V power resource should ramp VDD_MCU 0.5ms before all 0.8V core level supplies.
- VDDAR_CPU or VDDAR_CORE supplies cannot be grouped with 0.85V VDD_MCU since they must ramp-up after VDD_CORE & VDD_CPU supplies.
- VDDAR_MCU & VDD_MCU_WAKE1 supply can be grouped with 0.85V VDD_MCU power resource.

TPS6594133A PMIC + TPS389006004 SVS Cold Boot-up Timing for PDN-3x

Leo PMIC-A, PN TPS6594133ARWERQ1 (TI PN ID = 1, MP Buck Rails = 2, PG2.0 NVM ID = 3A Rev 5)
HCPS-A & B, Tulip PN TPS62873Y1QWRXSRQ1 (15A PN ID = 3, Jacinto7 Family ID = Y1)
Safety Voltage Supervisor, PN TPS389006004RTERQ1 (OTP ID = 004 = new common PN for use with J7 PDN-3x scheme)

Rev	Date	By	Desc
V0.1	5/21/2022	BMc	Initial capture of PMIC & SVS device initialization sequences vs SoC power up seq & release to active operations.
V0.2	5/24/2022	BMc	Updated SVS operation & added SVS PG set-up time margin calculations to ensure positive margin wrt PMIC's GPIO unmasking for MAIN & MCU_PWRGRP_PG/IRQn signaling at cold power up seq
V0.3	5/31/2022	BMc	Updated following 3 rd PMIC & SVS power seq review
V0.4	6/2/2002	BMc	Updated 1. Functional opr of SVS device begins after OTP, BIST & I2C Addr completion (i.e. Pwr Seq timer, LF VMON) 2. Auto-Mask opr to includes masking of IRQn & SLEEPn pins and aligns to 1x Pwr Seq timer reg value
V0.5	6/30/2022	BMc	Increased Auto-Mask elapsed time-out from 5 to 15ms to ensure no false positives
V0.6	8/31/2022	BMc	Added "PMIC_ColdBOOT_#" power up step elapsed time stamps wrt VSYS_3V3 ramping up vs SoC PORz release to begin system SW boot.
V0.27	11/20/2024	BMc	1. Updated PMIC PN NVM revision from v4 to v5 2. Added PFSM's 1 st state "Wait for Enable" that is NVM defined, NVM 133A requires 5.5ms max for capturing desired PDN settings based upon VCCA input voltage auto-detecting 3.3 or 5V



SVS IRQn Opr Margin = Auto-Mask timeout – Last supply ramp-up
SVS nom & PMIC nom:
16 – (8.5+0.5) = 7.0ms (positive margin needed)
SVS min & PMIC max (+/-5% OTP/NVM times):
15.2 – (9+0.5) = 5.7ms (positive margin needed)

<u>Date</u>	<u>Rev</u>	<u>By</u>	<u>History</u>
V0.22	10/13/2023	BMc	<u>PDN Diagram updates:</u> 1. Captured proposed SCH 7 PCB vE5 updates that will change the SVS-A & SVS-B supply connections from “Always ON” VCCA = VSYS_3V3 to “PDN controlled” power rails as shown & per new note #13 2. Added new PDN-3G diagram with 3G vs 3A change list summary 3. Added new PDN-3M diagram with 3M vs 3A change list summary
V0.23	10/25/2023	BMc	<u>PDN Diagram updates:</u> 1. Updated PMIC PN NVM to v4 2. Added sub-bullet a) to Note 3.3 B) addressing early enabling of discrete LDSW-A, LDO-E & LDO-F during temporary development & debug when Rup is installed to GPIO_9/EN_3V3_VIO net. 3. Changed SVS-A VDD supply to use VDD_MCUIO_3V3 (same as SVS-B) & updated Note #13 with an explanation. 4. Added PDN-3G & PDN-3M variants to show Grouped MCU & Main scheme with rail groups & reduced power components.
V0.23c	12/06/2023		5. Changed SVS-A & -B device ACT connections to VDD supplied by VDD_MCUIO_3V3 power rail and updated Note #13 with explanation. <u>PMIC SVS Pwr Seqs:</u> 1. Increase time btw pwr up seq Time Step #2 vs #3 to add 0.5ms margin btw VDD_MCU_0V85 vs VDD_CORE_0V8 for worst case per SoC errata i2406s
V0.23b	10/27/2023		2. Updated PMIC PN NVM revision from v2 to v4
V0.23c	12/06/2023		3. Added new power up seq constraints list for quick reference as needed to align with Errata i2406 “IO Glitches during Pwr Up Seqs”
V0.24	5/20/2024	BMc	<u>PDN Diagram updates:</u> 1. Removed in-line ferrite bead filters from VDA_DLL_0V8 connections to SoC’s VDDA_OP8_xxx analog supply inputs since filtering of the LDO power resource is not needed. Aligns PDN diag to match latest EVM SCH & board (PROC141E5). 2. Update VPP_EFUSE_1V8 LDO PN from 300mA TLV73318-Q12 to 500mA TPS7A2118P-Q1 to support robust J7xxx Efuse programming. Aligns PDN diag to match latest EVM SCH & board (PROC141E5)
V0.25	6/25/2024	BMc	<u>All PDN Diagram updates</u> 1. Updated PMIC 133A NVM rev to v5 per RTM planned revision <u>PDN-3G & -3M only</u> 1. Changed SVS-A & -B supply connection from VDD_MCUIO_3V3 to VDD_GPIORET_3V3 due to Grouped PDN net name change sourced from same PMIC LDO2 Vout. This will enable SVS asserted IRQ to be reset upon PMIC trying a cold boot. <u>PMIC NVM Rev History</u> 1. Updated PMIC ‘133A Rev History to align with slide set updates.
V0.26	7/30/2024	BMc	<u>PDN-3F Diag only</u> 1. Updated WKUP_I2C0 pull up supply from VDD_GPIORET_3V3 previously supplying VDDSHV0_MCU on PDN-3A to VDD_MCOIO_3V3 no supplying VDDSHV0_MCU on PDN-3F. <u>PDN-3G Diag only</u> 1. Updated H_MCU_INTn_1V8 pull up supply from VDD_MCUIO_1V8 previously supplying VDDSHV2_MCU on PDN-3A/F to VDD_IO_1V8 no supplying VDDSHV0_MCU on PDN-3G/M. 2. Updated H_MCU_PORz_1V8 & H_SOC_PORz_1V8 pull up supplies from VDA_MCU_1V8 previously supplying MCU’s VDDA_WKUP on PDN-3A/F to VDA_PLL_1V8 now supplying MCU’s VDDA_WKUP on PDN-3G/M. <u>PDN-3M Diag only</u> 1. Updated WKUP_I2C0 pull up supply from VDD_GPIORET_3V3 previously supplying VDDSHV0_MCU on PDN-3G to VDD_IO_3V3 no supplying VDDSHV0_MCU on PDN-3M. 2. Updated H_MCU_INTn_1V8 pull up supply from VDD_MCUIO_1V8 previously supplying VDDSHV2_MCU on PDN-3A/F to VDD_IO_1V8 no supplying VDDSHV0_MCU on PDN-3G/M. 3. Updated H_MCU_PORz_1V8 & H_SOC_PORz_1V8 pull up supplies from VDA_MCU_1V8 previously supplying MCU’s VDDA_WKUP on PDN-3A/F to VDA_PLL_1V8 now supplying MCU’s VDDA_WKUP on PDN-3G/M.
V0.27	10/31/2024	BMc	<u>All PDN Diagram updates</u> 1. Updated discrete buck’s ENABLE input connections to more accurately show the 20k resistor located in-line with a single, low voltage translator output. 2. Updated Note 9, example #2 text & diag to show 20k resistor in-line with buck’s ENABLE inputs. <u>TPS6594133A PMIC + TPS389006004 SVS Cold Boot-up Timing for PDN-3x</u> 1. Added cold boot-up timing diag with engineering notes
V0.28	12/11/2024	BMc	<u>PDN-3F Diag only</u> 1. Corrected a copy & paste error by changing net name “DSRT_PWRGRP_IRQn” connected to SVS-A’s IRQ pin to “MAIN_PWRGRP_IRQn”.
V0.29	2/7/2025	BMc	<u>PDN-3G & -3M Diags only</u> 1. Fixed power rail connections to OSPI memories by correctly changing name from VDD_MCUIO_1V8 to VDD_IO_1V8 for Grouped PDN scheme. <u>PDN-3F Diag only</u> 2. Added Note 14 to clarify removal of SVS-B & MCU_PWRGRP_IRQn board level net due to removing GPIO Retention low power mode. <u>PMIC SVS Pwr Seqs:</u> 1. Corrected power up seq timing diagram to correctly show time btw pwr up seq Time Step #2 vs #3 as only 0.5ms (instead of 1.0ms) per PMIC 133A’s v4 update & as captured in v0.23 changes above.

<u>Date</u>	<u>Rev</u>	<u>By</u>	<u>History</u>
V0.16	7/28/2022	BMc	<u>PDN Diagram updates:</u> 1. Replaced discrete “OR Gate” FET logic circuitry with 1x Bit Configurable Multi-Function gates in 4x places
V0.17	8/31/2022	BMc	<u>PMIC SVS Pwr Seq v0.6 updates:</u> 1. Following Power Seq diag & PMIC NVM setting updates Added “PMIC_ColdBOOT_#” power up step elapsed time stamps wrt VSYS_3V3 ramping up vs SoC PORz release to begin system SW boot.
	9/2/2022	BMc	<u>PDN Diagram updates:</u> 1. Update Note #9 to clarify open-drain interface is needed for automotive grade, single channel voltage translator. 2. Added “Modular PDNs support Flexible Feature Sets” table for reference 3. Removed net “H_MAIN_WKOn” connected to SoC output “PMIC_WAKEOn” since it’s only needed if Main GPIO Retention low power mode is used. 4. Connect PU R on SEL_SDIO_3V3_1V8n signal to VDD_IO_3V3 supply instead of VCCA_3V3 to avoid current bleed into SOC GPIO during power up seq.
V0.18	11/30/2022	BMc	<u>PDN Diagram updates:</u> 1. Fixed PMIC NVM value in PN Breakdown from “13” to “3A” and in block diag from “20” to “3A”. Added latest revision # of NVM 3A as “Rev 2”. 2. Clarified Note 9 for low voltage translator options and the open-drain interface stage need for TPS6287x-Q1 Enable/Status bi-dir pin. 2. Reverting “OR gate” enabling discrete LDO supplying VDD1_DDR_1V8 to original discrete FET OR gate circuit (see Note 12 for details). 3. Updating PMIC PN NVM to rev2 for optimizations that simplifies & adds flexibility in using 1x common PN for multiple PDN types. 4. Updated Tulip Buck (TPS62873Y1-Q1) supply connections to control logic input pins to align with EVM SCH details & buck data sheet.
V0.18b	2/06/2023	BMc	<u>PDN Diagram, SoC Pwr Seq & PMIC SVS Pwr Seq updates:</u> 1. Fixed PMIC NVM ID typos & minor clarifications to PDN Diag, Rev 18 history text 2. Added “TPS6594133A NVM Rev History” slides for easy reference.
V0.19	2/15/2023	BMc	<u>PDN Diagram updates:</u> 1. Added Do Not Install & Blue-wire/New connection as SCH/BOM updates needed for PMIC NVM “133A” Rev 2 optimizations. 2. Update Note #3 to clarify existing board SCH/BOM revisions for “133A” Rev 2.
V0.19b	2/20/2023	BMc	<u>PDN Diagram updates:</u> 1. Fixed PMIC NVM ID & Rev# update on pwr regulator sub-block & GPIO8's assigned “GPI” function change per NVM rev2 update
V0.20	2/21/2023	BMc	<u>PDN Diagram updates:</u> 1. Removed legacy buffer & Watchdog disable switch control that are no longer needed when using optimized PMIC NVM Rev2 or higher. This shows a “clean” diag recommended for new board designs. 2. Updated J784S4 Processor block to show Pkg Code, Wake Logic desc, “blue font” high-lighting diff vs TDA4AL/VL/VM (J721S2).
V0.21	9/8/2023	BMc	<u>PDN Diagram updates:</u> 1. Updated optional “Disable Watch-Dog” control for production optimized Leo PMIC NVM rev 4 that enables WDOG Timer by default so disabling WDOG Timer for development & debugging tasks needs an optional pull-up resistor connected to GPIO9 as shown. 2. Updated PDN Note #3 accordingly. 3. Added new PDN-3F diagram with 3F vs 3A change list summary <u>PMIC NVM Rev Hist updates:</u> 1. Added NVM Rev4 Summary of Changes
V0.22	10/13/2023	BMc	<u>PDN Diagram updates:</u> 1. Captured proposed SCH 7 PCB vE5 updates that will change the SVS-A & SVS-B supply connections from “Always ON” VCCA = VSYS_3V3 to “PDN controlled” power rails as shown & per new note #13 2. Added new PDN-3G diagram with 3G vs 3A change list summary 3. Added new PDN-3M diagram with 3M vs 3A change list summary

<u>Date</u>	<u>Rev</u>	<u>By</u>	<u>History</u>
V0.14	5/19/2022	BMc	<p>PDN Diag updates:</p> <ol style="list-style-type: none">Revised Safety Voltage Supervisor (SVS) scheme due to IRQn asserting low during power up seq can not be cleared without SW I2C writes.<ol style="list-style-type: none">Changed SVS-A & -B PN to enable an open drain PG output from nRESET pin.Shuffled supply rail connections to SVS-A & -B to align voltage levels to same MON# inputs for potentially defining 1x SVS PN for -A & -BRenamed MAIN_PWR_GRP_IRQn to MAIN_PWR_GRP_PG & connect to SVS-A's PG/nRESET pin & tri-state buffer feeding PMIC GPIO_8Renamed MCU_PWR_GRP_IRQn to MCU_PWR_GRP_PG & connected to SVS-B's PG/nRESET pin.Isolated Tulip enable using new EN_CPU_CORE_VDD control, connected Tulip open drain PG to new MAIN_PWRGRP_PG netRenamed nets connected to discrete LDOs to new MAIN_PWRGRP_PG & MCU_PWRGRP_PG nets <p>PMIC SVS Pwr Seqs (added new timing diagram)</p> <ol style="list-style-type: none">Initial capture of PMIC & SVS device initialization sequences vs SoC power up seq & release to active operations.
V0.14a	5/24/2022	BMc	<p><u>PMIC SVS Pwr Seqs:</u></p> <p>Updated SVS operation & added SVS PG set-up time margin calculations to ensure positive margin wrt PMIC's GPIO unmasking for MAIN & MCU_PWRGRP_PG/IRQn signaling at cold power up seq</p>
V0.14b	5/31/2022	BMc	Updated following 3 rd PMIC & SVS power seq review
V0.14c	6/2/2002	BMc	Updated <ol style="list-style-type: none">Functional opr of SVS device begins after OTP, BIST & I2C Addr completion (i.e. Pwr Seq timer, LF VMON)Auto-Mask opr to includes masking of IRQn & SLEEPn pins and aligns to 1x Pwr Seq timer reg value
V0.14c	6/23/2022	BMc	<p><u>PDN Diagram updates:</u></p> <ol style="list-style-type: none">Shuffled supply rail connections to SVS-A & -B to align voltage levels to same MON# inputs for potentially defining 1x SVS PN for -A & -BShow PG outputs from discrete bucks & LDOs as optional signals not required since SVS-A & SVS-B are providing VMON OV/UV coverage.
V0.14d	6/30/2022	BMc	<ol style="list-style-type: none">Added existing MCU power rails sourced from PMIC that have desired voltage levels to satisfy “unused” SVS-B VMON inputs to enable 1x common PN for SVS-A & -B while avoiding false positives on MCU_PWRGRP_IRQn.Updated SVS-A 7 -B to show new common PN for use with Jacinto7 J784S4 PDN-3A scheme as shown below. <p><u>PMIC SVS Pwr Seqs:</u></p> <ol style="list-style-type: none">Increased Auto-Mask elapsed time-out from 5 to 15ms to ensure no false positives
V0.15	7/25/2022	BMc	<p><u>PDN Diagram updates:</u></p> <p>Following PDN diag & PMIC NVM setting updates are needed as a result of power up & down seq bench testing:</p> <ol style="list-style-type: none">PMIC NVM settings for GPIO5 will need to revert from Open-Drain to Push-Pull buffer type to correctly control signaling. This works since the EN_GPIO_RET signal (sourced from GPIO5) only interfaces to 2x low voltage FETs with Vth ~1.0.Add “AND” gate to control disabling of dual output LDO supplying VDD_SD_VIO. This will disable VDD_SD_DV voltage whenever EN_3V3_VIO is low as needed to remove power during low power modes (MCU Only, DDR_RET & GPIO_RET). <p><u>PDN Pwr Seq updates:</u></p> <p>Following Power Seq diag & PMIC NVM setting updates are needed as a result of power up & down seq bench testing:</p> <ol style="list-style-type: none">Updated power down seq of VDA_DLL_OV8 to shift disabling from 2.5ms to 1.0ms due to ~1ms delay in VDA_DLL_OV8 RC discharge before VDD_CPU_AVS & VDD_CORE_OV8 are disabled by VDA_DLL_OV8 dropping below 0.6V FET Von threshold.Updated power down seq of VDD_MCU_OV85 to shift disabling from 2.5ms to 2.0ms to ~align with disabling of VDD_CPU_AVS & VDD_CORE_OV8.
V0.16	7/28/2022	BMc	<p><u>PDN Diagram updates:</u></p> <ol style="list-style-type: none">Replaced discrete “OR Gate” FET logic circuitry with 1x Bit Configurable Multi-Function gates in 4x places
V0.17	8/31/2022	BMc	<p><u>PMIC SVS Pwr Seq v0.6 updates:</u></p> <ol style="list-style-type: none">Following Power Seq diag & PMIC NVM setting updates Added “PMIC_ColdBOOT_#” power up step elapsed time stamps wrt VSYS_3V3 ramping up vs SoC PORz release to begin system SW boot.
	9/2/2022	BMc	<p><u>PDN Diagram updates:</u></p> <ol style="list-style-type: none">Update Note #9 to clarify open-drain interface is needed for automotive grade, single channel voltage translator.Added “Modular PDNs support Flexible Feature Sets” table for referenceRemoved net “H_MAIN_WK0n” connected to SoC output “PMIC_WAKE0n” since it's only needed if Main GPIO Retention low power mode is used.Connect PU R on SEL_SDIO_3V3_1V8n signal to VDD_IO_3V3 supply instead of VCCA_3V3 to avoid current bleed into SOC GPIO during power up seq.

<u>Date</u>	<u>Rev</u>	<u>By</u>	<u>History</u>
V0.1	12/11/2021	BMc	PDN Diag updates: 1. Initial capture J784S4 (AHP) EVM PDN starting from J721S2 (AEP) EVM Dual Leo + Hera Interim PDN-0A v1.4
V0.2	1/7/2022	BMc	1. Reassigned PMIC LDO4 to create “EN_MCU_VIO” control signal and added discrete LDO to supply VDD_PLL_1V8 previously supported by LDO4. This is due to 100% PMIC GPIO assignments.
V0.3	1/9/2022	BMc	1. Completed 1 st draft PDN diag
V0.4	1/11/2022	BMc	1. Updates captured during SCH capture & design. Initial capture of pwr seqs beginning with latest NVM settings for J721S2 PDN. 2. Updates per IPM Team (Leo PMIC) team fdbk from (Jaco v, email 1/11/2022). 3. Updates per VSR Team (Greenland SVS) team fdbk from (Mathew J, email 1/11/2022). 4. Updates per LV-BSR (Tulip Buck) team fdbk (Nigel S, email 1/13/2022).
V0.5	1/18/2022	BMc	Updated power up seq for J784S4 PDN-3A
V0.6	1/20/2022	BMc	PDN Diag updates: 1. Changed discrete LDO PN suppling VDA_PLL_0V8 from TLV73318P-Q1 to TPS745xxP-Q1 to gain 2x types of CL & PG status. To be reviewed with FuSa engineers. 2. Cleaned up engineering notes & captured PDN Notes for key items. 3. Inverted polarity of MAIN_PWRGRP_IRQn to be asserted high logic at PMIC GPIO input in order to easily combine multiple signals on common GPIO_8 input, see Note 3. Pwr Seqs updates: 1. Verified standard power down seq steps & groups is applicable.
V0.7	1/28/2022	BMc	Updated during 2nd NVM settings review
V0.8	2/6/2022	BMc	PDN Diag updates 1. SVS connections following detailed reviews with VRS team. 2. Cleared a few design notes & plan to address remaining notes this week.
V0.9	3/3/2022	BMc	PDN-3A Diag updates 1.Updated SVS nSLEEP control signals as follows: Main SVS-A connect EN_3V3_VIO to nSLEEP input; MCU SVS-B connect VDD_MCUIO_3V3 to nSLEEP. 2. Removed R-Muxes showing alternative, EVM test mode only connecting MCU_GPIORET 0.8V & 3.3V supplies to Main domain supplies New PDN-3B Diag captured 3. Added PDN-3B diag to show supported reduced PDN scheme when Retention low power modes & optional end product features are not desired. Note, no impact to PDN power rail timing seqs.
V0.10	3/9/2022	BMc	Created “ Detailed EVM...PDN-3A” specific PDN diagram from v0.10 to show provisioned alternative connections for EVM optional testing & to meet EVM requirements 1. Add 4x R-Muxes to enable all GPIO_RET test modes: Standard (no GPIORET), MCU_GPIORET, MAIN_GPIORET & combined MCU&MAIN_GPIORET Update All PDN Diags as follows: 2. Updated net names to Q7 & Q9 from EN_GPIO_RET to revised name EN_GPIO_RET_3V3 aligned to GPIO_5's OD output with PU resistor to 3.3V supply. 3. Replace inverter on MAIN_PWRGRP_INTn with tri-state Buffer & OE connected to H_MCU_PORz to “Time-Mux” vs “Wire-Mux” w/ btw WDOG_DISABLE. 4. Updated “NOTES” & added “SoC Input Supply to Power Rail Groupings vs PDN Low Power Mode Features” table
V0.11	3/14/2022	BMc	PDN-3A Diag updates: 1. Fixed “H_WKUP_I2C0” pull-up supply to correctly show “VDD_MCU_GPIORET_3V3” which SCH uses since WKUP I2C0 interface is ref to vddshv0_mcu 2. Updated SVS PN to show Catalog PN will be used for initial wakeup boards & to support OTP definition & testing of custom PDN-3A OTP PN.1. Pwr Seqs updates: 1. Updated power rail general descriptions (blue text in middle of diag) to align with assigned name
V0.12	3/31/22	BMc	PDN-3A Diag updates: 1. Changed Tulip buck Vin supply from VCCA_3V3 to VSYS_3V3 per worst case analysis (see new Note #10) to reduce PMIC Safety FET voltage drop & improve margins on all 3.3V power rails supplied by VCCA_3V3 (I.e. Load Switches supplying SoC’s VDD_IO_3V3 & VDD_MCUIO_3V3).
V0.13	4/4/2022	BMc	PDN-3A Diag updates: 1. Added voltage translation to MCU_PORz_1V8 for DIR control of Tri-State Buffer creating MAIN_PWRGRP_IRQn_BUF signal on PMIC GPIO_8. 2. Updaed Note 9 to show 2x options for single bit, low voltage translation components.